

REMARKS

To address the indefiniteness rejection of claim 18, claim 17 has been amended to note that it is a diode-connected NMOS transistor that is coupled into the second feedback path as shown, for example, in Figure 3b. Claim 18 has been amended to refer to the second transistor in the second feedback path as set forth in claim 15. Accordingly, claim 18 is now definite.

Claim 20 has been rewritten into independent form to include "a first feedback path having a first transistor with a gate terminal coupled to the output node and with a second terminal coupled to a ground node to determine one of the voltage thresholds" and "a second feedback path having a second transistor with a gate terminal coupled to the output node and with a second terminal coupled to a power supply voltage node to determine a remaining one of the voltage thresholds." Applicants note that the second feedback path is plainly supported by the P2 transistor of Figure 6 whereas the first feedback path is supported by the N2 transistor of this figure. The limitation of "at least one diode coupled to a path selected from the first feedback path and the second feedback path such that an on-current through the selected path is reduced as a supply voltage for the Schmitt trigger is reduced" is supported by P3. The second inverter has been amended such that "a first terminal of the second transistor couples to the output terminal of the first inverter," which is supported by P2 of Figure 6. Accordingly, claim 20 is not misdescriptive.

In addition, claims 1 and 15 were amended to address minor informalities.

Applicants respectfully traverse the rejection of claims 1 - 4, 6 - 8, and 10 - 18 as being anticipated by the Tailliet reference (USP 6,549,048). Applicant notes that claim 1 recites "at least one diode coupled to a path selected from the first feedback path and the second feedback path such that an on-current through the selected path is reduced as a supply

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voltage for the Schmitt trigger is reduced." Through this innovation, the feedback paths may include large transistors (as is desired for higher supply voltages) yet these large transistors will desirably act as small transistors as the supply voltage is decreased.

Transistor T302 of Figure 3 is asserted to satisfy such an inventive claim limitation. However, transistor T302 is not a diode-connected transistor – as discussed by Tailliet in Col. 5, lines 9-30, T302 is connected in a current-mirror configuration with T21. In turn, T21 is driven by a current I. As I increases, the current through T302 increases proportionally depending upon the relative dimensions of T21 and T302. Thus, T302 is plainly not a diode-connected transistor – an example of which is provided by Tailliet as transistors T20 and T21 because their gate and drain are tied together (Col. 4, lines 14-16).

Applicants further note that it is the source (not the drain) of T302 that is grounded. The drain is plainly isolated from node E2/E3 that controls the voltage on the gate of T302. Accordingly, claim 1 and its dependent claims are abundantly patentable over the Tailliet reference. Claims 12 and 15 (and their dependent claims) are patentable for analogous reasons.

Applicants respectfully traverse the rejection of claims 5, 9, and 20 as being obvious over Tailliet for the same reasons discussed with regard to the anticipation rejections.

Accordingly, Applicants respectfully submit that the pending claims are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited.

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If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

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Respectfully submitted,



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